Abstract of the Disclosure

An image processing apparatus and a method for implementing picture-in-picture with frame rate conversion are provided. The image processing apparatus includes an input buffer unit, a data synchronizing unit, first through third memories, and a memory control unit. The input buffer unit buffers input data which are externally and asynchronously input through two or more channels by different input clock signals and outputs buffered data as first data and first data enabling signals. The data synchronizing unit synchronizes the first data output from the input buffer unit with an output clock signal in response to the input clock signals and the first data enabling signals and outputs synchronized data as second data and second data enabling signals in response to each of the first data enabling signals. The first memory multiplexes the second data according to time sharing, stores the second data in different regions, and outputs stored data in response to a first memory enabling signal. The second memory writes and reads data output from the first memory in response to a frame buffer control signal. The third memory stores data output from the second memory and outputs stored data as a display signal in response to a second memory enabling signal. The memory control unit controls data flow between the first memory and the second memory, frame rates of the first and second input data and the display signal in the second memory, and data flow between the second memory and the third memory.

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